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# Reduction of Multipliers in FIR Filter Using Various Algorithms-Review

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## Abstract

Due to the explosive growth of digital signal processing applications, the demand for high performance and low power is getting higher and higher.Finite-impulse response digital filters(FIR) are one of the most widely used devices in DSP systems.In signal processing applications,multiplier plays the major role.Increase in multipliers leads to increase in area,delay and power.Several algorithms have been proposed to reduce the multipliers in FIR filter using various techniques.Some of the approaches are Fast FIR Algorithm,Iterated Short Convolution Algorithm,Common Sub-Expression Algorithm and Distributed Architecture Algorithm.The multiplers can be reduced drastically by using few adders which are weak operations when compared to multipliers.By increasing few adders more number of multipliers can be reduced and the parameters area, delay and power can also be reduced significantly.This article discuss the various algorithms to the reduction of multipliers in FIR filter.

**Keywords**: Finite-impulse-response (FIR) filter, Fast FIR Algorithm(FFA),Common Sub-Expression Algorithm(CSE),Iterated Short Convolution Algorithm(ISC),Distributed Architecture Algorithm(DA)

## Introduction

Finite-impulse response(FIR) digital filters are one of the most widely used devices in DSP systems.Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation.The aim is to reduce the number of multipliers at the expense of adders to reduce area,delay and power.Exchanging multipliers with adders is advantageous because adders weigh less than multipliers interms of area and they do not increase along with the length of the filter,whereas the multipliers increases along with the length of the filter.

Fast FIR Algorithm(FFA) proposes new parallel FIR filter architectures which are beneficial to symmetric coefficients interms of hardware cost.This structure exploit the inherent nature of symmetric coefficients reducing half the number of multipliers at the expense of adders.FFA has the applications ranging from wireless communication to video and image processing.

Common Sub expression Elimination (CSE) algorithm is based on the Canonical Signed Digit (CSD) representation of filter co-efficient for implementing low complexity FIR filters. The CSE algorithm is used to find and eliminate more common sub expressions among filter co-efficient which results in power and area saving while implemented in FIR filters.

According to the Iterated Short Convolution (ISC)Algorithm we usually first derive smaller length fast parallel filters and then cascade or iterate them to design parallel FIR filters with long block sizes. This algorithm is combined with fast two and three point convolution algorithms to get the general iterated short convolution algorithm (ISCA).

In Distributed arithmetic Algorithm, the MAC operations are replaced by a series of LUT access and summations. It is a one way to implement convolution with multiplier less unit. The basic idea is to replace all multiplications and additions by a table and a shifter-accumulator. one way to implement convolution with multiplier less unit.They are used in various applications such as telecommunication,Application Specific Integrated Circuits (ASIC) and Field-Programmable Gate Arrays (FPGA) platforms and others. This article discuss the various algorithms to the reduction of multipliers in FIR filter.

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## Materials and methods

**Fast FIR Algorithm(FFA)**

Mou and Duhamel, (1991) [1] proposed a Short-length FIR filters with reduced arithmetic complexity where all multiplications are replaced by decimated subfilters based on a multiply-accumulate (MAC) structure using Fast FIR Algorithm. These algorithms retain partially the FIR filter structure,while reducing the arithmetic complexity. They allow various tradeoffs between structural regularity and arithmetic efficiency. This flexibility in the algorithms derivation allows finding the best possible solution in any type of implementation. The process can be reiterated on the subfilters, the short-length filters are recognized as the basic building tools of these fast algorithms. some improvements in the number of additions by recognizing that FIR filtering, seen as a running process, involves a pseudocirculant matrix instead of a general Toeplitz one. Using this pseudocirculant presentation,we can very easily derive the transposed version of all fast FIR filtering algorithms.

Tsao and Choi (2010) [2] proposed a new parallel FIR filter structures based on FFA consisting of polyphase decompositions by utilizing the symmetry of coefficients.This structure exploits the nature of even symmetric co-efficients and save a significant amount of multipliers at the expense of adders.A set of symmetric coefficients would only require half the filter length of multiplications in a single FIR filter , which is similar to the fact that half the number of multiplications in the single subfilter block can be reused for the multiplications of whole taps. Therefore the total amount of saved multipliers would be the number of subfilter blocks that contain symmetric coefficients times half the number of multiplications in a single subfilter block.

Tsao and Choi (2012) [3] proposed the design for symmetric convolutions based on odd length and provide the new parallel FIR filter structures consisting of polyphase decomposition which can further reduce amounts of multipliers required in the subfilter section by exploiting the inherent nature of the symmetric coefficients using FFA technique. This proposed new structures exploit the nature of symmetric coefficients of odd length and further reduce the amount of multipliers required at the expense of additional adders.

Selvakumar and Bhaskar (2012) [4] proposed a parallel FIR filter structure based on FFA technique consisting of polyphase decomposition has been implemented using carry save and ripple carry adder for further optimization. The aim is to design an efficient FFAs for parallel FIR filter structure with the constraint that the filter tap must be a multiple of 2. The reduction in area complexity is achieved by eliminating the bulky multiplier with an adder called ripple carry and carry save adder. Here we provide a new parallel FIR filter structure based on FFA, which can reduce amounts of bulky multiplications in the sub-filter section by exploiting the inherent nature of the symmetric coefficients.

Karthikeyan and Saravanan (2013) [5] proposed a distributed arithmetic algorithm based new parallel Linear Phase FIR filter architectures based on fast FIR algorithms (FFAs), which are beneficial to symmetric convolutions in terms of the hardware cost. This proposed new structures exploit the nature of symmetric coefficients of odd length and further reduce the amount of multipliers required at the expense of additional adders.The architecture is implemented using spartan3E family device XC3S500E using Modelsim 5.7 and Xilinx 9.2i. This can be done at 200MHz with core power of 175 mW and consumes 2008 LUTs and 682 FFs.

Arathy and Krishnapriya (2013) [6] proposed a linear phase FIR digital filters based on two contributions. First, the structure is based on fast FIR algorithm (FFA) that utilizes the symmetry of coefficients thereby reducing half the number of multipliers in the sub filter section at the expense of adders. After the modified FIR filter design using distributed Arithmetic (DA) is used for multiplier-less implementation of DSP systems. It replaces all multiplications and additions by a lookup table (LUT) and a shifter-accumulator thereby it can save considerable amount of hardware resources.

Shikha et al., (2014) [7] proposed a low power area efficient digital filters to reduce dynamic power consumption based on fast FIR algorithms (FFAs) using polyphase decomposition technique, that requires minimum number of multipliers and low power adders. Generally multipliers consume more power and larger area than the adders. The FIR filter was synthesized and implemented using Xilinx ISE V10.1 and Virtex IV FPGA to target device xc3s250e.

Ramya and Manohar (2014) [8] proposed a parallel FIR filter structures for symmetric convolutions Based on Fast FIR Algorithm(FFA) by using carry select adder(CSA).Here the CSA are used instead of normal adders (full adder and ripple carry adder)

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because they take more time to execute the program. The simulation result are observed in modelsim6.4b simulator and synthesized by using Xilinx ISE tool.

**Common SubExpression Algorithm(CSE)**

Mahesh and Vinod (2008) [9] proposed a Low-Complexity Higher Order Digital Filters based on New Common Subexpression Elimination Algorithm using binary representation of coefficients for the implementation of higher order FIR filters with a fewer number of adders. This proposed binary-coefficient method offers good reduction in the number of adders in realizing higher order filters.This can be achieved without much increase in critical path length of filter coefficient multipliers. The goal of CSE is to identify multiple occurrences of identical bit patterns that are present in the CSD representation of coefficients and to eliminate these redundant multiplications to minimize the number of logical operators.

Thenmozhi and Kirthika (2012) [10] proposed an efficient architecture for reconfigurable FIR Filter architectures based on common subexpression elimination(CSE) Algorithm using two new approaches namely Constant Shift Method (CSM)and Programmable Shift Method (PSM). The complexity of linear phase FIR filters is dominated by the number of adders (subtractors) in the coefficient multiplier. The CSE algorithm reduces number of adders in the multipliers and dynamically reconfigurable filters can be efficiently implemented .By using CSM and PSM methods with fixed number of multipliers the complexity can be reduced by applying the greedy CSE algorithm.

Joyprincy et al., (2013) [11] proposed a reconfigurable FIR digital filter architecture based on Common Sub-expression Elimination (CSE) algorithm by providing mathematical analysis of the power saving and filter performance degradation approach to reduce the dynamic power of the FIR filter. The CSE algorithm reduces the number of adders in the multipliers and then dynamically reconfigurable filters can be efficiently implemented**.** The filter is dynamically reconfigured by changing the filter order and the order is changed by turning of the multiplier whose inputs are mitigate to be eliminated**.**

Geethalakshmi and Jayamathi (2013) [12] proposed a low complexity linear phase FIR filter based on CSE algorithm using Minimum Signed Powers-of Two (MNSPT) or Canonical Signed Digit (CSD) representation technique of the multiplier. This can be implemented using a series of shifts and additions or subtractions. The CSE algorithm is used to find and eliminate more common sub expressions among filter co-efficient which results in power and area saving while implemented in FIR filters.

Edmund et al., [13] proposed a low complexity FIR filters based on greedy Common Subexpression Elimination (CSE) algorithm with a look-ahead method based on the Canonic Signed Digit (CSD) representation of filter coefficients. The number of adders can be reduced by choosing the maximum number of frequently occurring common subexpressions using look-ahead algorithm. This adder reduction is achieved without any increase in critical path length.

Martínez-peiró et al., [14] proposed a multiplierless FPGA FIR filter design based on new Signed Common Subexpression Elimination algorithm (SCSE) using RAM-based FPGA technology and compared with distributed arithmetic implementation approach. Here the subexpressions are not shared between coefficients, thereby allowing a reduction in the logical depth of the final structure. The structure of the filter obtained from the algorithm can be easily HDL described. The method can be generalized to be used in different matrix vector multipliers.

**Iterated Short Convolution (ISC)Algorithm**

Chao Cheng and Keshab K. Parhi (2004) [15] proposed a hardware efficient fast parallel FIR filter structure based on Iterated Short Convolution (ISC) algorithm using mixed radix algorithm and fast convolution algorithm.The structure can be transposed to obtain a fast parallel FIR filter and the number of required additions is dependent on the order of iteration. The order for short convolutions should be 4x4, 3x3 and 2x2 and this will lead to the lowest implementational cost**.** This ISC based algorithm facilitates automatic hardware implementation of parallel FIR filters, which is very efficient when the filter coefficients or the level of parallelism change, especially when the length of the FIR filter and the level of parallelism are large.

Chao Cheng and Keshab K. Parhi (2005) [16] proposed a low complexity parallel FIR filter structures. First, the FIR filter is transformed into linear convolution, which is then implemented by Iterated Short Convolution algorithm. The structure for FIR filter is used as a processing core to implement the subfitlers of proposed parallel FIR filter structures**.** we can develop an efficient core to share the computation of all these subfilters in different time slots, we can save a lot of hardware

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cost.To transform N-tap FIR into NxN linear convolution, which generate N FIR filter outputs in just 1 clock cycle. The hardware cost will depend on the complexity of the NxN linear convolution and additional N-1 additions and N-1 delay elements are also required.The L-parallel N-tap FIR filter can be generalized as,Form an ISC based FIR filter; Replace the subfilters with a core (N/L)x(N/L) linear convolution and two delay element matrices to arrange the input and output of the (N/L)x(N/L) linear convolution. Finally, implement (N/L)x(N/L) linear convolution using the iterated short convolution algorithm.

Chao Cheng and Keshab K. Parhi (2007) [17] proposed a 2-stage parallel FIR filter structures based on iterated short-convolution algorithm (ISCA) using Cook–Toom or Winograd algorithm. Here the subfilters in the parallel FIR structures are replaced by a second stage parallel FIR filter.These structures can efficiently reduce the number of required multiplications and additions at the expense of delay elements**.** Generally the parallel FIR filter has many subfilters of the same length and structure and they require most of the overall hardware cost of the parallel FIR filters.By utilizing these features and developing a second stage parallel FIR filter as a shared processing core we can reduce the hardware cost of the overall parallel FIR filter design.

**Distributed Architecture (DA)Algorithm**

Vigneswaran and Subbarami (2007) [18] proposed a high speed FIR filters based Dynamic Distributed Algorithm(DDA) using adders,look up tables(LUT) and shifters.The algorithm eliminates the multiplier unit which requires more number of adders.The implementation translates to L multiplications and L-1 additions per sample to compute the result using Multiply Accumulate(MAC)engine.It will require L-MAC cycles,before the next input sample is processed.It uses the sharing of combinational logic blocks(CLBs) and embedded multipliers.For DDA method,we decompose all the constant multiplications into additions,LUTs and shifts and optimized the expressions using the same algorithm.Xilinx SpartanIII devices is used for optimization.

Ramesh and Nathiya (2012) [19] proposed an efficient implementation of Finite Impulse Response Filter (FIR) using Distributed Arithmetic (DA) architecture. The DA based technique consists of look up table (LUT), shift registers and scaling accumulator.Here, the multipliers in FIR filter are replaced with multiplierless DA based technique which is implemented using Distributed Arithmetic which consists of look up table and then partitioning is involved. Analysis on the performance of various filter orders with various partitions are done using Xilinx synthesis tool.

Badave and Bhalchandra (2012) [20] proposed a multiplierless FIR filter implementation based on area efficient distributed arithmetic technique.In this method the precomputed values of inner product are stored in LUT, which are added and shifted with number of iterations equal to the precision of input samples. The LUT is sliced into desired number because the size of LUT grows exponentially with the order of the filter. This sliced LUT-DA scheme on an FPGA consists of input registers, sliced LUT units and the shifter/accumulator unit and it would require an adder tree to perform addition of partial products.

## Results and discussion

**Fast FIR Algorithm(FFA)**

Mou et al.,(1991) result shows that this algorithm not only compute more efficiently moderate- to long-length FIR filtering on DSP's**,** but also more efficiently compute short-length(<64**)**FIR filtering when considering the total number of operations. Tsao et al., (2010) concluded that the significant amount of multipliers are saved at the expense of few adders interms of hardware cost using even and odd symmetric coefficients. Bhaskar et al.,(2012) result shows that this algorithm reduces the hardware complexity by approximately by 10%. Karthikeyan et al.,(2013) result shows that this algorithm is used to reduce the convolution multipliers in the FIR Filter Architecture by exploiting the nature of symmetric coefficients of odd length. Arathy et al.,(2013) result shows that this technique replace all multiplications and additions by a look up table (LUT) and a shifter-accumulator thereby it can save considerable amount of hardware resources and it consumes less power and area.Shikha et al., (2014) result shows that this algorithm consumes low power area efficient digital filters and reduce the dynamic power consumption of FIR filter.It reduces more multipliers and can reduces more system cost. Ramya et al., (2014) result shows that this technique exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of adders. Since multipliers outweigh adders interms of hardware cost, and it is profitable to exchange multipliers with adders.

**Common SubExpression Algorithm(CSE**)

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Mahesh et al.,(2008) result shows that the binary-coefficient based CSE method offers good reduction in the number of adders in realizing higher order filters.This method offers an average adder reduction of 18% over the best known CSE method, without any increase in the logic depth.It is best suited for the implementation of higher order FIR filters. Thenmozhi et al.,(2012) result shows that the reconfigurable architectures can be easily modified to employ any common subexpression elimination (CSE) method, which results in architectures that offers good area and power reductions and speed improvement reconfigurable FIR filter implementations. Joyprincy et al., (2013) result shows that this algorithm reduces number of adders in the multipliers and dynamically reconfigurable filters can be efficiently implemented.Using this technique we can achieve power savings up to 41.9% with less than around 5.34% of area overhead with very graceful degradation in the filter output. Jayamathi et al., (2013) result shows that this method is used to find and eliminate more common sub expressions among filter co-efficient which results in power and area saving while implemented in FIR filters. Edmund et al., concluded that this algorithm offers an average adder reduction of about 20%. Martínez-peiró et al., concluded that this algorithm offers the best relation area – frequency operation, or number of adders - logical depth.

**Iterated Short Convolution (ISC)Algorithm**

Chao Cheng et al., (2004) concluded that the hardware efficient fast parallel FIR filter structure is very efficient in reducing hardware cost, when the length of the FIR filter is very large.Chao Cheng et al.,(2005) result shows that the low complexity parallel FIR filter structures is used to further reduce the hardware complexity.For a 576-tap FIR filter, when the parallelism level changes from 12 to 72, this algorithm can save 1755 to 3375 multiplications at the cost of 21 to 4658 additions and 1516 to 4749 delay elements.With the increase of throughput, we can save more number of multiplications at the cost of less and less delay elements. Chao Cheng et al.,(2007) result shows that this technique leads to significant hardware savings because the hardware cost of a delay element is only a small portion of that of a multiplier.By developing a second stage parallel FIR filter as a shared processing core ,then the hardware cost of the overall parallel FIR filter design can be reduced.

**Distributed Architecture Algorithm**

Vigneswaran et al., (2007) result shows that this algolrithm is used to achieve up to 56.75% reduction in the number of slices,upto 75% reduction in flipflops and up to 53.2% reduction in the number of LUTs and the speed of 31% can be improved . Ramesh et al.,(2012) result shows that this algorithm provides an efficient area-time-power implementation which involves significantly less latency and less area-delay complexity. Badave et al.,(2012) result shows that the design implementation and synthesis result shown that the improvement in speed of operation as well as saving in area, with more number of slices can be achieved. Highly flexible nature of this structure, allow it to use in complete serial to full parallel form.

## Conclusion

This review article illustrates how various algorithms are used to the reduction of multipliers in FIR filter.Multiplier plays the major role in DSP systems and they are the major portions in hardware consumption for the parallel FIR filter implementation. By increasing few adders more number of multipliers can be reduced and the parameters area, delay and power can also be reduced significantly.The applications of FIR filters are ranging from wireless communication to video and image processing.. This article will provide knowledge about various algorithms and techniques to the reduction of multipliers.

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